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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,167	01/13/2004	Shunpei Yamazaki	0553-0393	3564

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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,167	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/19/05, 8/4/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed July 19, 2005.

Response to Amendment

The amendment of claim 14 is sufficient to overcome the rejections of claims 14 and 15 under 35 U.S.C. 112, second paragraph stated in the previous office action. Therefore, these rejections are withdrawn.

Specification

The abstract of the disclosure is objected to because "reduces" should be changed to "reduced" (last line). Correction is required. See MPEP § 608.01(b).

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 13, 16, 17, 20, 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. (US 6,362,507, previously cited) in view of Jacobson et al. (US 6,294,401, previously cited).

Regarding claim 13, Ogawa discloses forming a gate electrode (202-204) over a substrate (201) having an insulating surface, laminating a semiconductor layer (209), a channel protection layer (219-222), and a semiconductor layer (214-218/223-230/233-234/239-240) having one of n-type or p-type conductivity over the gate electrode, forming a pixel electrode (250/272) and forming source or drain wirings (243-247) over the semiconductor layer having the n-type or p-type conductivity (col. 9, ln. 11 – col. 11, ln. 67). Ogawa discloses that the gate electrode, the

source/drain wirings and pixel electrodes are formed by sputtering instead of by discharging conductive material. Like Ogawa, Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the gate electrode, the source/drain wirings and additional circuit components by discharging material comprising conductive nanoparticles and performing a heat treatment of the nanoparticles by a heat lamp or laser (col. 5, ln. 51 – col. 7, ln. 10). Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate, source/drain layers and additional circuit components overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging and annealing method of Jacobson to form the gate, source/drain wiring layers and pixel electrodes of Ogawa because Jacobson teaches that by using the nanoparticles, the problems of harsh and wasteful fabrication conditions can be overcome.

Regarding claims 16, 20 and 24, Ogawa discloses that the conductive layer is formed semiconductor device can be incorporated into a display device (col. 21, ln. 60 – col. 22, ln. 5).

Regarding claim 17, Ogawa discloses forming a plurality of gate wirings and gate electrodes (202-204) over a substrate (201), forming an insulating film (207/208) over the gate wirings, laminating a plurality of semiconductor layers (209), a plurality of channel protection layers (219-222), and a plurality of semiconductor layer (214-218/223-230/233-234/239-240) having one of n-type or p-type conductivity over the gate electrode, forming a plurality of pixel electrodes (139/144) arranged in a matrix form over the substrate, and forming a plurality of source wirings (243-247) over the semiconductor layers having the n-type or p-type conductivity such that the source wirings extend across the gate wirings (col. 9, ln. 11 – col. 11, ln. 67). Ogawa discloses that wirings and electrodes are formed by sputtering instead of by discharging conductive material. Like Ogawa,

Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the wirings and the electrodes by discharging material comprising conductive nanoparticles and performing a heat treatment of the nanoparticles by a heat lamp or laser. Each formation of nanoparticles can have its own heat treatment step. Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate, source/drain layers and additional circuit components overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging and annealing method of Jacobson to form the wirings and electrodes of Ogawa because Jacobson teaches that by using the nanoparticles, the problems of harsh and wasteful fabrication conditions can be overcome.

Regarding claim 21, Ogawa discloses forming a plurality of gate wirings and gate electrodes (202-204) over a substrate (201), forming an insulating film (207/208) over the gate wirings, laminating a plurality of semiconductor layers (209), a plurality of channel protection layers (219-222), and a plurality of semiconductor layer (214-218/223-230/233-234/239-240) having one of n-type or p-type conductivity over the gate electrode, forming a plurality of pixel electrodes (139/144) arranged in a matrix form over the substrate, forming a plurality of source wirings (243-247) over the semiconductor layers having the n-type or p-type conductivity such that the source wirings extend across the gate wirings, and forming a second insulating film (249) over the source wirings (col. 9, ln. 11 – col. 11, ln. 67). Ogawa discloses that wirings and electrodes are formed by sputtering instead of by discharging conductive material. Like Ogawa, Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the wirings and the electrodes by discharging material comprising conductive nanoparticles and performing a

heat treatment of the nanoparticles by a heat lamp or laser. Each formation of nanoparticles can have its own heat treatment step. Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate and source/drain layers overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging and annealing method of Jacobson to form the wirings and electrodes of Ogawa because Jacobson teaches that by using the nanoparticles, the problems of harsh and wasteful fabrication conditions can be overcome.

Claims 14, 15, 18, 19, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. (US 6,362,507) in view of Jacobson et al. (US 6,294,401) as applied to claims 13, 17 and 21 above, and further in view of Speakman (US 6,713,389, previously cited).

Regarding claims 14, 15, 18, 19, 22 and 23, Ogawa and Jacobson do not disclose the pressure at which the first, second and third conductive materials are formed. Like Jacobson, Speakman discloses a method of forming conductive wirings of a semiconductor device by depositing droplets of a liquid conductive mixture on the surface of the substrate. Speakman teaches that it is advantageous to form the conductive droplets in a reduced pressure atmosphere because in higher pressures, the droplets will become deformed which impairs its dimensional stability and placement accuracy (col. 40, ln. 10-14). Speakman states that the reduced pressure atmosphere can be in the range of 1×10^{5} to 1×10^{-6} N/m^2 (Pa) (col. 4, ln. 6-28). At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit the conductive wirings and electrodes of Ogawa in a reduced pressure atmosphere because Speakman teaches that

the reduced pressure provides better dimensional stability and better placement accuracy of the wirings and electrodes.

Claims 25, 28-32, 35-39, 42-46 and 49-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (JP 2001-052864) in view of Jacobson et al. (US 6,294,401).

Regarding claim 25, Yamazaki discloses forming a semiconductor island (302) over a substrate (300), forming an insulating film (311) over the island, forming a gate electrode (312-316) and a gate wiring (335), doping an impurity element having a n-type or p-type conductive type into the island using the gate electrode as a mask, forming an interlayer insulating film (336) over the gate electrode, forming source and drain wirings (337-343) over the interlayer insulating film and forming a first electrode (349) over the source and drain wirings (Fig. 3-5, Abstract, paragraphs 109-156). Yamazaki discloses forming an electroluminescent layer by using an ink-jet discharge technique, but discloses forming the gate and wiring layers by sputtering. Like Yamazaki, Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the wirings and the electrodes by discharging material comprising conductive nanoparticles and performing a heat treatment of the nanoparticles by a heat lamp or laser. Each formation of nanoparticles can have its own heat treatment step. Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate and source/drain layers overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging and annealing method of Jacobson to form the wirings and electrodes of Yamazaki because Yamazaki teaches using a discharge method to deposit the electroluminescent layer and because Jacobson teaches that by using the discharging method of

depositing the wiring and electrodes, the problems of harsh and wasteful fabrication conditions can be overcome.

Regarding claims 28, 35, 42 and 49, Yamazaki discloses that the semiconductor device can be incorporated into a display device (paragraphs 263-268).

Regarding claims 29, 36, 43 and 50, Yamazaki discloses forming an electroluminescent layer by discharging a fourth conductive material and forming a second electrode over the electroluminescent layer. Yamazaki does not disclose the specific method used to deposit the second electrode. Like Yamazaki, Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the wirings and the electrodes by discharging material comprising conductive nanoparticles. Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate and source/drain layers overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging method of Jacobson to form the wirings and electrodes of Yamazaki because Yamazaki teaches using a discharge method to deposit the electroluminescent layer and because Jacobson teaches that by using the discharging method of depositing the wiring and electrodes, the problems of harsh and wasteful fabrication conditions can be overcome.

Regarding claims 30, 37, 44 and 51, Yamazaki discloses that the semiconductor island is initially made of amorphous silicon (paragraphs 111-112).

Regarding claims 31, 38, 45 and 52, Yamazaki discloses that the first electrode is an anode electrode (paragraph 146).

Regarding claim 32, Yamazaki discloses forming a semiconductor island (302) over a substrate (300), forming an insulating film (311) over the island, forming a gate electrode (312-316)

and a gate wiring (335), doping an impurity element having a n-type or p-type conductive type into the island using the gate electrode as a mask, forming an interlayer insulating film (336) over the gate electrode, forming source and drain wirings (337-343) over the interlayer insulating film and forming a first electrode (349) over the source and drain wirings (Fig. 3-5, Abstract, paragraphs 109-156). Yamazaki discloses forming an electroluminescent layer by using an ink-jet discharge technique, but discloses forming the gate and wiring layers by sputtering. Like Yamazaki, Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the wirings and the electrodes by discharging material comprising conductive nanoparticles from an ink-jet unit and performing a heat treatment of the nanoparticles by a heat lamp or laser. Each formation of nanoparticles can have its own heat treatment step. Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate and source/drain layers overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging and annealing method of Jacobson to form the wirings and electrodes of Yamazaki because Yamazaki teaches using a discharge method to deposit the electroluminescent layer and because Jacobson teaches that by using the discharging method of depositing the wiring and electrodes, the problems of harsh and wasteful fabrication conditions can be overcome. Jacobson does not specifically teach that the number of ink-heads provided in the ink-jet unit used to deposit the first electrode is larger than that provided in the ink-jet unit used to deposit the gate electrode. However, Jacobson teaches that the ink-jet unit may include multiple heads (col. 6, ln. 3-10). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use more ink-heads to form the first electrode

than are used to form the gate electrode because the first electrode covers an area of the substrate that is many times larger than the area of the substrate covered by the gate electrode.

Regarding claim 39, Yamazaki discloses forming a plurality of semiconductor islands (302) over a substrate (300), forming an insulating film (311) over the islands, forming a plurality of gate electrodes (312-316) and gate wirings (335), doping an impurity element having a n-type or p-type conductive type into the island using the gate electrode as a mask, forming an interlayer insulating film (336) over the gate electrodes, forming a plurality of source and drain wirings (337-343) over the interlayer insulating film and forming a plurality of first electrodes (349) arranged in matrix form over the source and drain wirings (Fig. 3-5, Abstract, paragraphs 109-156). Yamazaki discloses forming an electroluminescent layer by using an ink-jet discharge technique, but discloses forming the gate and wiring layers by sputtering. Like Yamazaki, Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the wirings and the electrodes by discharging material comprising conductive nanoparticles from an ink-jet unit and performing a heat treatment of the nanoparticles by a heat lamp or laser. Each formation of nanoparticles can have its own heat treatment step. Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate and source/drain layers overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging and annealing method of Jacobson to form the wirings and electrodes of Yamazaki because Yamazaki teaches using a discharge method to deposit the electroluminescent layer and because Jacobson teaches that by using the discharging method of depositing the wiring and electrodes, the problems of harsh and wasteful fabrication conditions can be overcome.

Regarding claim 46, Yamazaki discloses forming a plurality of semiconductor islands (302) over a substrate (300), forming an insulating film (311) over the islands, forming a plurality of gate electrodes (312-316) and gate wirings (335), doping an impurity element having a n-type or p-type conductive type into the island using the gate electrode as a mask, forming an interlayer insulating film (336) over the gate electrodes, forming a plurality of source and drain wirings (337-343) over the interlayer insulating film and forming a plurality of first electrodes (349) arranged in matrix form over the source and drain wirings (Fig. 3-5, Abstract, paragraphs 109-156). Yamazaki discloses forming an electroluminescent layer by using an ink-jet discharge technique, but discloses forming the gate and wiring layers by sputtering. Like Yamazaki, Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the wirings and the electrodes by discharging material comprising conductive nanoparticles from an ink-jet unit and performing a heat treatment of the nanoparticles by a heat lamp or laser. Each formation of nanoparticles can have its own heat treatment step. Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate and source/drain layers overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging and annealing method of Jacobson to form the wirings and electrodes of Yamazaki because Yamazaki teaches using a discharge method to deposit the electroluminescent layer and because Jacobson teaches that by using the discharging method of depositing the wiring and electrodes, the problems of harsh and wasteful fabrication conditions can be overcome. Jacobson does not specifically teach that the number of ink-heads provided in the ink-jet unit used to deposit the first electrode is larger than that provided in the ink-jet unit used to deposit the gate electrode. However, Jacobson teaches that the ink-jet unit may include multiple

heads (col. 6, ln. 3-10). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use more ink-heads to form the first electrode than are used to form the gate electrode because the first electrode covers an area of the substrate that is many times larger than the area of the substrate covered by the gate electrode.

Claims 26, 27, 33, 34, 40, 41, 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (JP 2001-052864) in view of Jacobson et al. (US 6,294,401) as applied to claim 25 above, and further in view of Speakman (US 6,713,389).

Regarding claims 26, 27, 33, 34, 40, 41, 47 and 48, Yamazaki and Jacobson do not disclose the pressure at which the first, second and third conductive materials are formed. Like Jacobson, Speakman discloses a method of forming conductive wirings of a semiconductor device by depositing droplets of a liquid conductive mixture on the surface of the substrate. Speakman teaches that it is advantageous to form the conductive droplets in a reduced pressure atmosphere because in higher pressures, the droplets will become deformed which impairs its dimensional stability and placement accuracy (col. 40, ln. 10-14). Speakman states that the reduced pressure atmosphere can be in the range of 1×10^{5} to 1×10^{-6} N/m^2 (Pa) (col. 4, ln. 6-28). At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit the conductive wirings and electrodes of Ogawa in a reduced pressure atmosphere because Speakman teaches that the reduced pressure provides better dimensional stability and better placement accuracy of the wirings and electrodes.

Response to Arguments

Applicant's arguments filed July 19, 2005 have been fully considered but they are not persuasive.

Regarding the rejection of claim 13, Applicant argues that Ogawa and Jacobson allegedly fail to teach the limitation of forming a pixel electrode by discharging a conductive material. Ogawa teaches forming pixel electrodes (250/272). Jacobson teaches that the TFT device of his invention can be connected to other printed components to form a functional circuit. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging and annealing method of Jacobson to form the electrodes of Yamazaki because Yamazaki teaches using a discharge method to deposit the electroluminescent layer and because Jacobson teaches that by using the discharging method of depositing the wiring and electrodes, the problems of harsh and wasteful fabrication conditions can be overcome.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
September 28, 2005

AMIR ZARABIAN
EXAMINER
TECHNOLOGY CENTER 2800